REMARKS

This paper is being provided in response to the Final Office Action mailed May 14, 2003, for the above-referenced application. In this response, Applicants have amended claims 1 and 17 to clarify that which Applicant considers to be the invention. Applicants respectfully submits that the amendments to the claims are fully supported by the originally-filed specification.

The rejection of claims 1-9 and 17-24 under 35 U.S.C. 112, first paragraph, is hereby traversed and reconsideration is respectfully requested. Applicants' claims, as amended herein, recite a delay circuit with a first delay section having a *frequency dependent delay time* based on said frequency variable clock signal and a second delay section with a fixed delay time independent of said frequency variable clock signal. Applicants respectfully submit that this feature is fully enabled by the specification and would be easily understood by one of ordinary skill in the art. As shown, for example, in Figure 10, Applicants describe a delay circuit 5 having a variable delay section 16 and a fixed delay section 9. (See page 20, lines 23-26). The fixed delay section 9 provides a *fixed delay time*, that is a predetermined delay time amount and, for example, the output of the fixed delay section can be an internal clock signal. The variable delay section 16 has a delay quantity which *depends on the frequency* of an external clock signal that provides the operating frequency. (See page 21, lines 1-27). Applicants respectfully submit that the concept of a delay section having a fixed delay time and a delay section having a delay time which depends on the operating frequency is adequately described and fully enabled by the specification as written. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 1-3, 7, 8, 9, 17-19 and 23 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,111,448 to Shibayama (hereinafter "Shibayama") is hereby traversed and reconsideration is respectfully requested.

Independent claim 1, as amended herein, recites a delay locked loop (DLL) circuit comprising a delay circuit which is connected to first and second nodes and which delays an original clock signal supplied to the first node based on a delay control signal. The delay circuit generates first to n-th (n is an integer more than 1) internal clock signals. The first internal clock signal is outputted from the second node. The internal clock signals other than the first internal clock signal are outputted from the delay circuit without passing through the second node and lead the first internal clock signal in phase by a predetermined phase value. The original clock signal is a frequency variable clock signal and the delay circuit includes a first delay section with a frequency dependent delay time based on the frequency variable clock signal and a second delay section with a fixed delay time independent of said frequency variable clock signal. A phase comparing circuit compares the original clock signal and the first internal clock signal and outputs a phase difference. A delay control circuit outputs the delay control signal to the delay circuit based on the phase difference outputted from the phase comparing circuit. Claims 2-9 depend directly or indirectly on claim 1.

Independent claim 17, as amended herein, recites a method of generating timing signals, comprising delaying an original clock signal supplied to a first node based on a delay control signal. First to n-th (n is an integer more than 1) internal clock signals are generated from the delayed original clock signal. The first internal clock signal is outputted from a second node and

the internal clock signals other than the first internal clock signal are outputted without passing through the second node and lead the first internal clock signal in phase by a predetermined value. The original clock signal is a frequency variable clock signal, and a first delay section with a frequency dependent delay time based on the frequency variable clock signal and a second delay section with a fixed delay time independent of the frequency variable clock signal control delay of the original clock signal and the internal clock signals. A phase difference between the original clock signal and the first internal clock signal is detected. The delay control signal is generated based on the detected phase difference. Claims 18-23 depend directly or indirectly on independent claim 17.

The Shibayama reference discloses a clock signal distribution circuit for distributing a clock signal at high speed and with less phase displacement on a large scale integrated circuit. The circuit utilizes two variable delay circuits, a clock tree, a control circuit and a phase comparison circuit.

Applicants' independent claims recite at least the features of a delay circuit for delaying the original clock signal and internal clocks signals that includes a first delay section with a *frequency dependent delay time based on the frequency variable clock* signal and a second delay signal with a *fixed delay time independent of the frequency variable clock signal.* With this feature, even if the frequency of the original clock signal is changed, the first delay section with frequency dependent delay generates a coarsely controlled clock signal and the second delay section with fixed delay generates the first internal clock signal, allowing other internal clock signals that lead the first internal clock signal in phase by a predetermined value to be generated.

Shibayama discloses a variable delay circuit and clock tree; however, the variable delay circuit has *no frequency dependency in the delay time*, as shown in Figure 8 and described in col. 7, line 64 to col. 8, line 28. Shibayama's variable delay circuit provides variable delay based on inputs D1 to D7 to inverters 61-67 and NAND gates 68-90. The inputs to D1 - D7 can either be a "1" or a "0" and depending on the distribution of these input values to D1 - D7, a delay from 2d to 16d (in units of 2d) is offered. Shibayama does not disclose the binary inputs to D1 - D7 as being dependent upon the operating frequency. Therefore, when the frequency of the original clock signal is changed, it would be difficult to control the phases of the delivered clock signal.

The Office Action states that delay time of the delay inherently depends upon the operating frequency. Applicants respectfully submit that is not the case, as for example, in the delay time configuration disclosed by Shibayama that discloses a variable delay that depends on the independently configurable binary inputs D1 - D7.

Applicants respectfully submit that Shibayama does not teach or suggest the features of a delay circuit for delaying the original clock signal and internal clocks signals that includes a first delay section with a *frequency dependent delay time based on the frequency variable clock* signal and a second delay signal with a *fixed delay time independent of the frequency variable clock signal*, as is claimed by Applicants. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 1-2, 17-19 and 23 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,642,082 to Jefferson (hereinafter "Jefferson") is hereby traversed and reconsideration is respectfully requested.

The features of Applicants' independent claims 1 and 17 are discussed above. Claims 2, 18, 19 and 23 depend therefrom.

The Jefferson reference discloses a loop circuit that includes circuitry for detecting when the output signal of the low-pass filter in the loop has either risen to a voltage which is relatively close to the power voltage of the circuit or has fallen to a voltage which is relatively close to the ground voltage of the circuit.

Applicants respectfully submit that Jefferson does not teach or fairly suggest at least the features of a delay circuit for delaying the original clock signal and internal clocks signals that includes a first delay section with a *frequency dependent delay time based on the frequency variable clock* signal and a second delay signal with a *fixed delay time independent of the frequency variable clock signal*, as is claimed by Applicants. Jefferson's variable delay circuit controls delay based on the voltage level of a VC signal. If the voltage of the VC signal is relatively high, the REFCLK signal will propagate through inverter stages faster than if the voltage of the VC signal is relatively low. Control based on the voltage level of a VC signal does not provide a *frequency dependent delay time based on the frequency variable clock signal.* Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 1-9 and 17-23 under 35 U.S.C. 103(a) as being unpatentable over Figure 9 of Applicant's admitted prior art (hereinafter "Applicant's APA") in view of Shibayama is hereby traversed and reconsideration is respectfully requested.

The features of Applicant's independent claims 1 and 17 are discussed above. Claims 2-9 and 18-23 depend therefrom.

Figure 9 of Applicant's APA discloses a conventional DLL circuit in which an intermediate output of a variable delay section 311 is taken out. Therefore, because the phase leading quantity to the final output has frequency dependence, an erroneous operation is caused. The conventional DLL circuit has no fixed time delay section.

The Shibayama reference is discussed above.

Applicants respectfully submit that neither Applicant's APA nor Shibayama teach or suggest the features of a delay circuit for delaying the original clock signal and internal clocks signals that includes a first delay section with a *frequency dependent delay time based on the frequency variable clock* signal and a second delay signal with a *fixed delay time independent of the frequency variable clock signal.*

Figure 9 of Applicant's APA, as discussed by Applicant, discloses that an intermediate output is taken out and that therefore, because the phase leading quantity to the final output has frequency dependence an erroneous operation is caused. Applicant's APA does not teach or

suggest two delay sections, one having variable delay and the other having fixed delay. Moreover, as noted by Applicant, the configuration of the intermediate output and final output causes the intermediate output to be out of phase. Applicant's APA does not provide any disclosure as to the specifics of an apparatus that could solve this problem. Applicant's later disclosure of the claimed invention includes the teachings of generating a clock signal with a predetermined preceding phase to an output signal without dependence on a used frequency. (See Summary of the Invention, page 13, lines 14-18). Applicants' respectfully submit that the Office Action is using improper hindsight reconstruction in applying Applicants' *own teachings* of how the claimed invention solves the above-noted problem against Applicants.

Accordingly, in view of the above, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Figure 1 of Applicant's APA in view of Figure 9 of Applicant's APA and further in view of Shibayama is hereby traversed reconsideration is respectfully requested.

Independent claim 24 recites a synchronous memory. A delay locked loop circuit delays an original clock signal supplied as an input. The delay locked loop circuit produces as an output a plurality of internal clock signals, a first of the plurality of internal clock signals being the original clock signal delayed by a first quantity and a second of the plurality of internal clock signals being the original clock signal delayed by a second quantity different than the first quantity. The delay locked loop includes a variable delay section with a frequency dependent

delay time that delays the original clock signal generated as a first delay signal based on a phase difference between the original clock signal and one of the plurality of internal clock signals. A fixed delays section that is a multi-stage structure of delay elements delays the first delay signal by a predetermined amount, the second internal clock signal being generated as an output of one of the stages. A logic circuit generates an enable signal in synchronism with the second internal clock signal and a latch signal in synchronism with the first internal clock signal. A memory section performs one of a read and write operation of data in response to the enable signal and latches the data for one of input and output to the memory section in response to the latch signal.

Figure 1 of Applicants' APA discloses the structure of a convention synchronous type DRAM composed of a DLL circuit, a logic circuit, and a memory section. The conventional DLL circuit does not include a frequency dependent delay section or a fixed delay section.

The Shibayama reference is discussed above.

Applicants respectfully submit that neither Figure 1 of Applicants' APA, Figure 9 of Applicants' APA, nor Shibayama, taken alone or in any combination, teach or suggest the feature of a variable delay section with a frequency dependent delay time...based on a phase difference between the original clock signal and one of the plurality of internal clocks signals and a fixed delay section that delays the first delay signal by a predetermined amount, as is claimed by Applicants.

Concerning Figures 1 and 9 of Applicants' APA, as noted above, Applicants respectfully submit that the Examiner is using improper hindsight reconstruction in applying Applicants' own teachings of the claimed invention against Applicants to solve the problem of non-coincident phases between internal and external clock signals in a DLL locked loop circuit and synchronous memory.

Applicants have recognized that in conventional synchronous type DRAM it is necessary to generate the second internal clock signal earlier than the internal clock signal synchronous with the external clock signal, but that it is not possible to carry out strict timing adjustment in a time width shorter than a half period of the external clock and therefore erroneous operation results. (See page 5, lines 8-22 and page 9, lines 1-8). Applicants' recognition of the above-noted problem and Applicant's solution to the problem according to the claimed invention should not be used against Applicants in deciding upon the patentability of the claimed invention. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 4-6 and 20-22 under 35 U.S.C. 103(a) as being unpatentable over Shibayama is hereby traversed and reconsideration is respectfully requested.

The features of Applicants' independent claims 1 and 17 are discussed above. Claims 4-6 and 20-22 depend therefrom.

As noted above, Applicants respectfully submit that Shibayama does not teach or suggest the features of a delay circuit for delaying the original clock signal and internal clocks signals

that includes a first delay section with a *frequency dependent delay time based on the frequency variable clock* signal and a second delay signal with a *fixed delay time independent of the frequency variable clock signal*, as is claimed by Applicants. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Figure 1 of Applicant's APA in view of Shibayama is hereby traversed and reconsideration is respectfully requested.

The features of Applicants' independent claim 24 are discussed above.

As noted above, Applicants respectfully submit that neither Shibayama nor Figure 1 of Applicants' APA, taken alone or in any combination, teach or suggest the features of a delay circuit for delaying the original clock signal and internal clocks signals that includes a first delay section with a *frequency dependent delay time based on the frequency variable clock* signal and a second delay signal with a *fixed delay time independent of the frequency variable clock signal*, as is claimed by Applicants. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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